

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS

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Serial No.
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Applicant(s)
Vorbach et al.

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January 14, 2004

Group Art Unit
2117

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,659,797	August 19, 1997	Zandveld et al.			
	5,844,422	December 1, 1998	Trimberger et al.			
	6,020,760	February 1, 2000	Sample et al.			
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	7,249,351	July 2007	Songer et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	1 061 439	December 20, 2000	EPO				
	WO 01/55917	August 2, 2001	PCT				
	WO 02/071196	September 26, 2002	PCT				

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	Bakkes, P.J., et al., "Mixing Fixed and Reconfigurable Logic for Array Processing," Dept. of Electrical and Electronic Engineering, University of Stellenbosch, South Africa, 1996 IEEE, pp. 118-125.
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		